What is claimed is:

1. A method for verifying a minimal level sensitive timing abstraction model, comprising:

extracting a plurality of parameters from a modeled circuit that includes sequential elements controlled by clock elements;

creating an echo-circuit that represents the plurality of parameters with nodes and time arcs, wherein the echo-circuit is lightweight and can be input into any static timing analysis (STA) tools, and wherein the echo-circuit enables a signal to propagate from an input port to an output port only if the signal arrives at the output port later than a clock signal from a most critical clock element controlling the output port;

identifying relevant timing paths in the echo-circuit, wherein the relevant timing paths are associated with the plurality of parameters;

identifying paths in the modeled circuit that connect sequential elements and correspond to the relevant timing paths in the echo-circuit; and

comparing the relevant timing paths in the echo-circuit with the corresponding paths in the modeled circuit.

2. The method of claim 1, wherein the extracting the plurality of parameters step includes extracting a required time parameter associated with a setup check node.

3. The method of claim 1, wherein the extracting the plurality of parameters step includes extracting a required time parameter associated with a hold check node.

4. The method of claim 1, wherein the extracting the plurality of parameters step includes extracting a valid time parameter associated with a dummy latch node, wherein the dummy latch node is controlled by the most critical clock element.

5. The method of claim 1, wherein the extracting the plurality of parameters step includes extracting a transparent delay arc parameter that represents a time delay a signal passes from an input port to an output port of the modeled circuit.

6. The method of claim 1, further comprising modifying names of the nodes in the echo-circuit to correspond to names of corresponding sequential elements in the modeled circuit.

7. The method of claim 1, further comprising generating an error report if the relevant timing paths in the echo-circuit do not match the corresponding paths in the modeled circuit.

8. The method of claim 1, wherein the creating the echo-circuit step includes creating a timing abstraction model that is port-based.

9. The method of claim 1, wherein the creating the echo-circuit step includes creating a timing abstraction model that has level triggered latches.

10. The method of claim 1, wherein the creating the echo-circuit step includes creating a timing abstraction model that is stimulus independent.

11. An apparatus for verifying a minimal level sensitive timing abstraction model, comprising:

means for extracting a plurality of parameters from a modeled circuit that includes sequential elements controlled by clock elements;

means for creating an echo-circuit that represents the plurality of parameters with nodes and time arcs, wherein the echo-circuit is lightweight and can be input into any static timing analysis (STA) tools, and wherein the echo-circuit enables a signal to propagate from an input port to an output port only if the signal arrives at the output port later than a clock signal from a most critical clock element controlling the output port;

means for identifying relevant timing paths in the echo-circuit, wherein the relevant timing paths are associated with the plurality of parameters;

means for identifying paths in the modeled circuit that connect sequential elements and correspond to the relevant timing paths in the echo-circuit; and

means for comparing the relevant timing paths in the echo-circuit with the corresponding paths in the modeled circuit.

12. The apparatus of claim 11, further comprising means for modifying names of the nodes in the echo-circuit to correspond to names of corresponding sequential elements in the modeled circuit.

13. The apparatus of claim 11, further comprising means for generating an error report if the relevant timing paths in the echo-circuit do not match the corresponding paths in the modeled circuit.

14. A computer readable medium providing instructions for verifying a minimal level sensitive timing abstraction model, the instructions comprising:

extracting a plurality of parameters from a modeled circuit that includes sequential elements controlled by clock elements;

creating an echo-circuit that represents the plurality of parameters with nodes and time arcs, wherein the echo-circuit is lightweight and can be input into any static timing analysis (STA) tools, and wherein the echo-circuit enables a signal to propagate from an input port to an output port only if the signal arrives at the output port later than a clock signal from a most critical clock element controlling the output port;

identifying relevant timing paths in the echo-circuit, wherein the relevant timing paths are associated with the plurality of parameters;

identifying paths in the modeled circuit that connect sequential elements and correspond to the relevant timing paths in the echo-circuit; and

comparing the relevant timing paths in the echo-circuit with the corresponding paths in the modeled circuit.

15. The computer readable medium of claim 14, further comprising instructions for modifying names of the nodes in the echo-circuit to correspond to names of corresponding sequential elements in the modeled circuit.

16. The computer readable medium of claim 14, further comprising instructions for generating an error report if the relevant timing paths in the echo-circuit do not match the corresponding paths in the modeled circuit.

17. The computer readable medium of claim 14, wherein the instructions for extracting the plurality of parameters step includes instructions for extracting a required time parameter associated with a setup check node.

18. The computer readable medium of claim 14, wherein the instructions for extracting the plurality of parameters step includes instructions for extracting a required time parameter associated with a hold check node.

19. The computer readable medium of claim 14, wherein the instructions for extracting the plurality of parameters step includes instructions for extracting a valid time parameter associated with a dummy latch node.

20. The computer readable medium of claim 14, wherein the instructions for extracting the plurality of parameters step includes instructions for extracting a transparent delay arc parameter that represents a time delay a signal passes from an input port to an output port of the modeled circuit.